PHY405 Lab 3

Friday, February 7, 2025

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Collaborators for all questions: none. Partner (for Lab 1-10): Jacob Villasana.

R-1

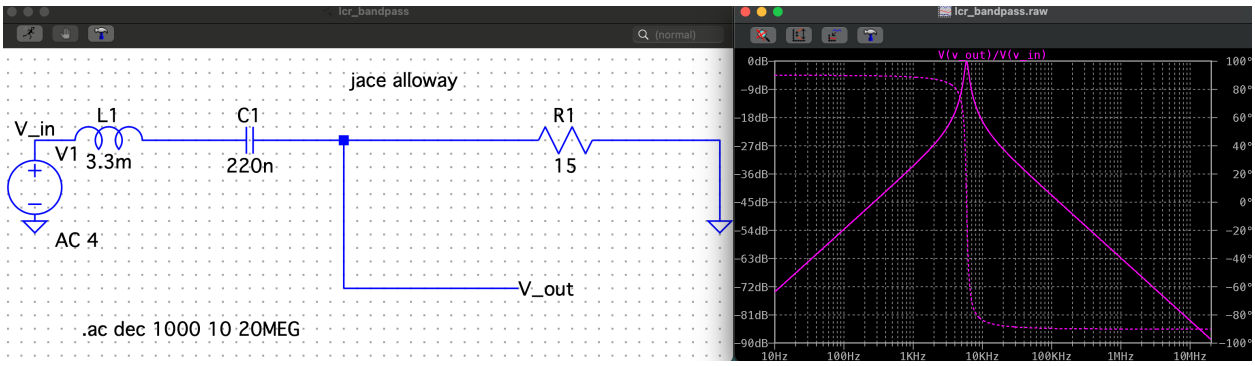

Figure 1: LTSpice circuit simulation of an LCR bandpass filter. AC input voltage was arbitrary. Initially, inductor, resistance, and capacitor values were different. After a lot of trial and error, this combination of components (which were available to us) yielded the appropriate cutoff frequency.

R-2

Methodology: Took some trial and error. Began with 100mH inductors at a base frequency of $f = 7$kHz. Used $f_0 = \frac{1}{2\pi}\frac{1}{\sqrt{LC}}$ to determine the capacitance C which yielded the appropriate cutoff. Initially with a 56Ω resistor, 100mH inductor, and 5nF capacitor. Peaks were repeatedly ~ -24dB. Moved to 10mH inductor, 47nF capacitor, and 15Ω resistor. Although the peak had moved up to ~ -6dB, which still wasn't best, the frequency was around 6.4kHz. The last attempt was to use a 3.3mH inductor with 15Ω resistor and 220μF capacitor, the peak shot up to ~ -2dB at a 6.4kHz cutoff which was in the 7 ± 1kHz range. Thus: the smaller the inductor in the LCR circuit the less attenuation at the peak.

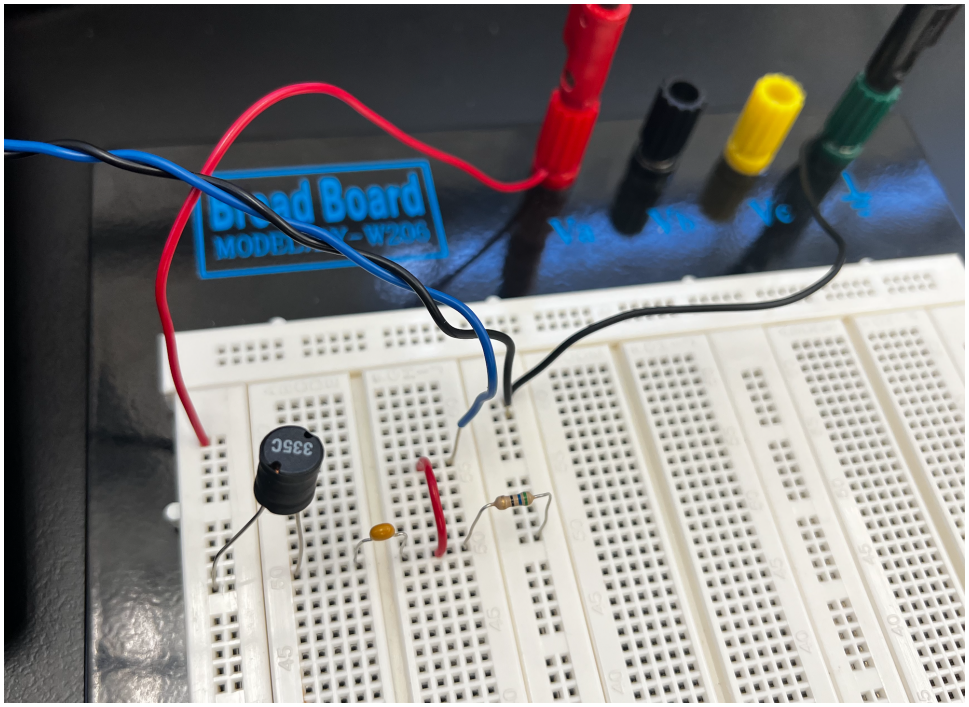

Figure 2: LCR bandpass circuit, created using a 3.3mH inductor, 15Ω resistor, and a 220μF capacitor.

R-3

Using the PyVisa control, a Bode plot of the circuit was created with the output voltage taken across the resistor.

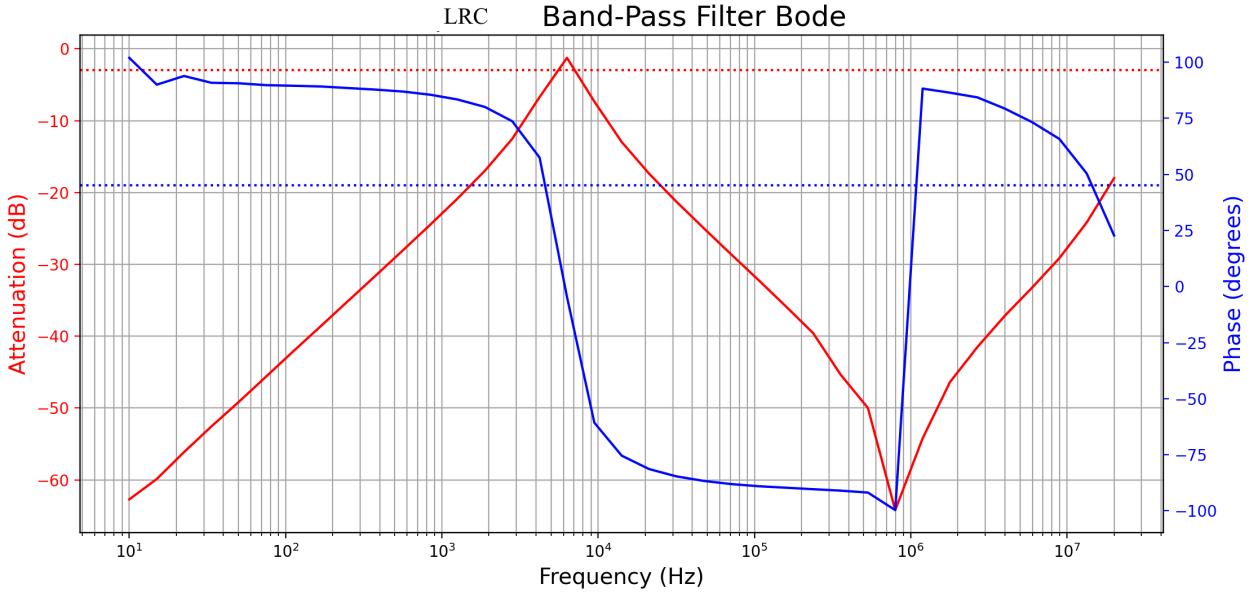

Figure 3: Bode plot generated from PyVisa and the oscilloscope of the circuit constructed in R1, R2. The peak of the bandpass is located at (-1.26 dB, 6.316 kHz).

R-4

Methodology: Note that the Bode plot generated by the oscilloscope is different than that of the LTSpice model. This is because the inductor in the circuit is not ideal. In LTSpice, the inductor used has zero internal resistance and parallel capacitance. However, if one were to select an inductor with a non-zero parallel capacitance/resistance, we would achieve a modelled Bode plot which is similar to that of the scope. In LTSpice, the Würth Electronik 744731332 WE-TIS 8075 capacitor was chosen (3.3mH, 6.2Ω series, 595kΩ parallel, 6.407pF capacitance).

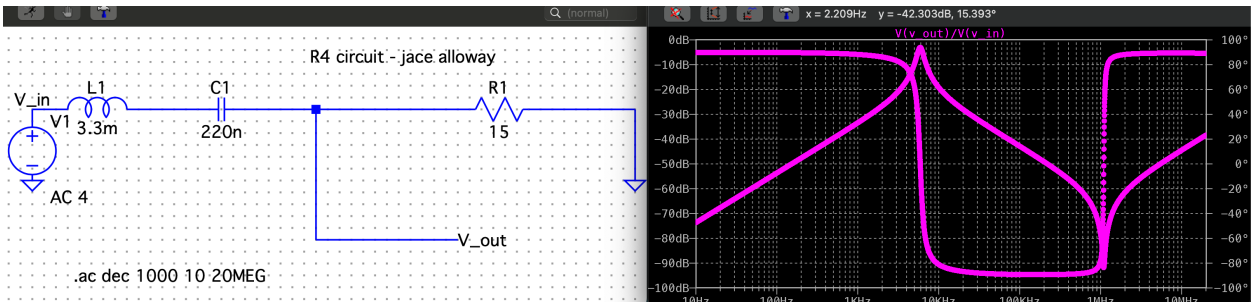

Figure 4: Bode plot of the modified LTSpice circuit, with a 3.3mH/6.407pF inductor instead of an ideal inductor.

R-5

Methology: Following the same principle as in R-4, the resistor and the inductor/capacitor series was swapped. Again using PyVisa, a Bode plot was generated on the oscilloscope:

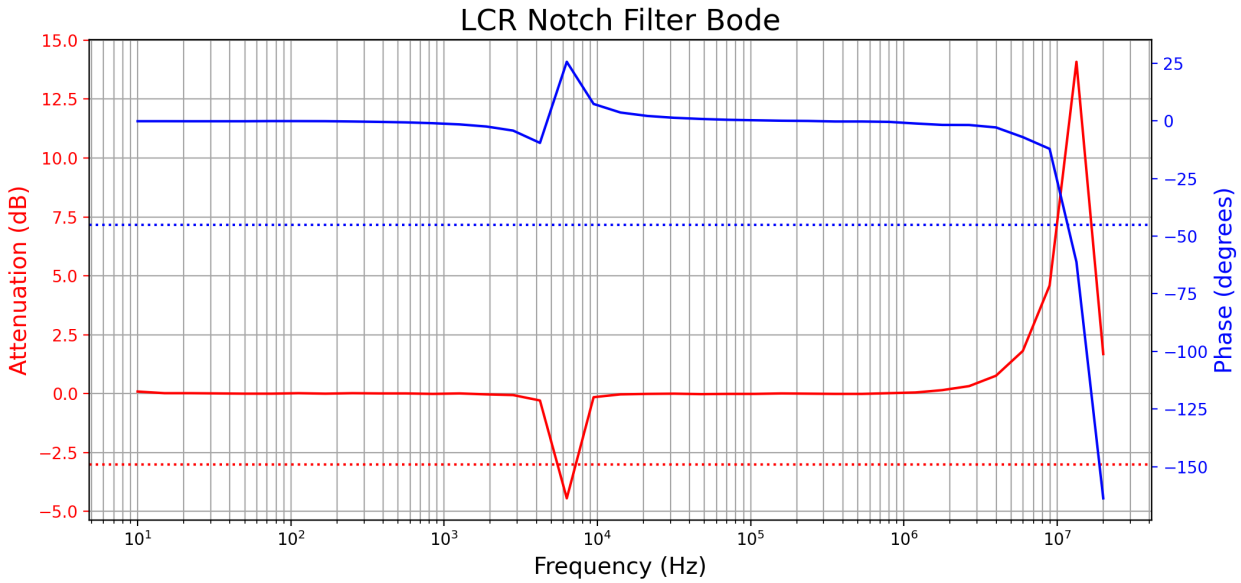

Figure 5: Bode plot of the notch filter circuit, with the swapping of the LC / R positions to obtain a notch filter.

We note that there is a spike in atttenuation around the 10MHz position, and this is because the inductor fails to attenuate at higher frequencies. Returning to LTSpice, the exact phenomenon was attempted to be re-created using all non-ideal parts, but it did not work and still had 0dB of

attenuation for higher frequencies in the model. Here, the same components were used as in R-4, but increasing the resistance (say, from 15Ω to 1kΩ) would deepen the attenuation at the 6kHz cutoff as mentioned in the lab manual.

R-6

Methodology: Using the multimeter (in series) and the DC power supply with a 3A current input, a blue LED and a 56Ω resistor, the voltage was varied and the DCA was measured on the ammeter. The data was imported into Python then plotted in matplotlib. Note that, $\log(e^x - 1)$ becomes linear as $x \to \infty$ but is initially logarithmic near 0. Taking the log (semilog plot on matplotlib) of the y-axis (the current), the data was identical to that of the model. Initially logarithmic, yet became linear as $V \to \infty$ *without* blowing the diode.

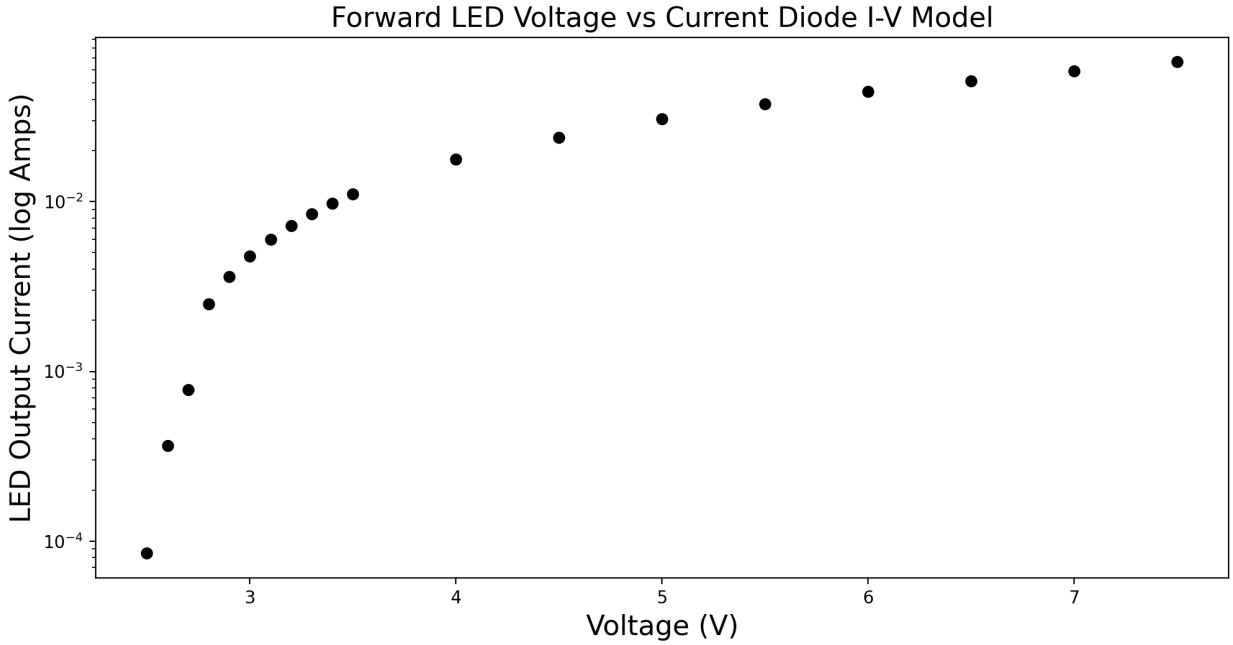

Figure 6: I-V diode model logarithmic plot of data recorded using an LED and resistor in series, a DCV power supply as 3A and an ammeter. Plotted on a semilog scale to isolate the linear behaviour as $V \to \infty$.

R-7

Methodology: A 1k resistor and a nominal 3.9V Zener diode were placed in series. The measured resistance using the multimeter was 0.98 ± 0.01kΩ, and the 3.9V Zener was measured to have a breakdown voltage of 2.98 ± 0.01V reverse, 0.70 ± 0.05V forward. The output voltage was taken across the diode. The oscilloscope was put in xy-mode. The resulting V-in and V-out relationship was displayed:

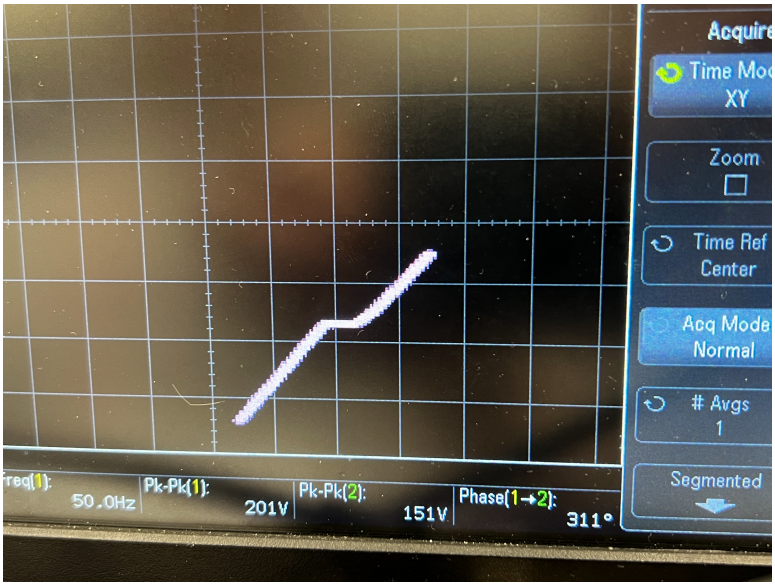

Figure 7: xy V-in and V-out relationship of a 3.9V Zener diode in a circuit with a 1k resistor.

Qualitatively, the upward slope on the right corresponds to the $0.3 - 0.7$V forward bias voltage (any forward voltage over 0.7V will force the PN junction to conduct), while the left downward slow corresponds to the *reverse* bias breakdown voltage, which is the voltage flowing opposite the diode until it conducts in the opposite direction. Thus Zener diodes can act as 'voltage regulators', limiting reverse and forward voltages.

R-8

Methodology: Initially, in LTSpice, a diode rectifier was designed (I didn't understand how rectifier diodes worked just yet when I designed this) by using 4 diodes. A capacitor was drawn over to the ground as an output-smoothing agent, including a 1k resistor. The 3.9V Zener was placed in reverse-bias mode to act as a 'voltage subtractor' to regulate output voltage. The schematic is shown below:

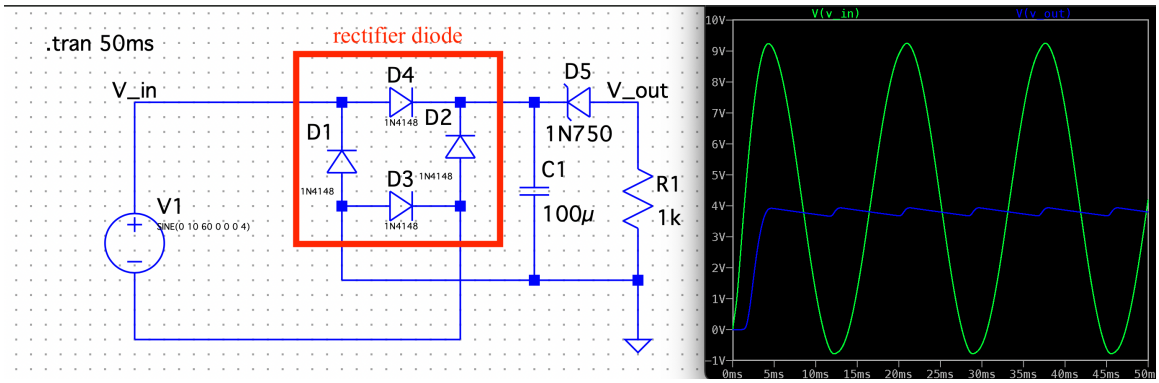

Figure 8: AC to DC voltage converter in LTSpice via explicit definition of the rectifier diode. The 100µ capacitor was arbitrarily chosen so that the best V-out smoothing was achieved. The Zener diode used in this circuit was 4.8V, not 3.9V

Eventually, in the lab, the 4-diode-loop-of-death was replaced with a single rectifier diode and the

circuit was constructed the exact same way, with the exception of grounding the negative input of the voltage connection (everything else remained the same). The exact schematic used in the lab is shown below.

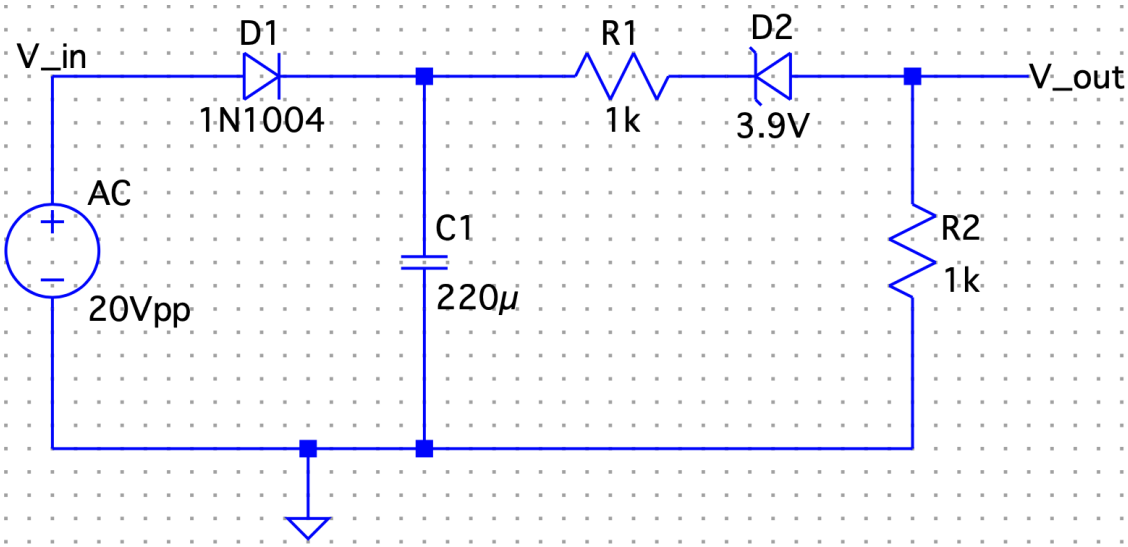

Figure 9: AC to DC voltage converter in LTSpice via implementation of the rectifier diode and the 3.9V Zener.

Over some trial and error, examining the output voltages across the final 1k resistor, it was found that adding a second resistor in front of / behind the Zener diode would reduce the current even more, which was helpful for regulating the output voltage. The higher the capacitor value, the greater the smoothing of the ripple. Hence from 100μ, a 220μF was chosen to reduce the rippler to be less than 5%. The multimeter was used to measure output DC voltage (DCV) and the ACV ripple compared to the approximate DCV. This was done just by probing wires into the circuit over V-out, as shown below.

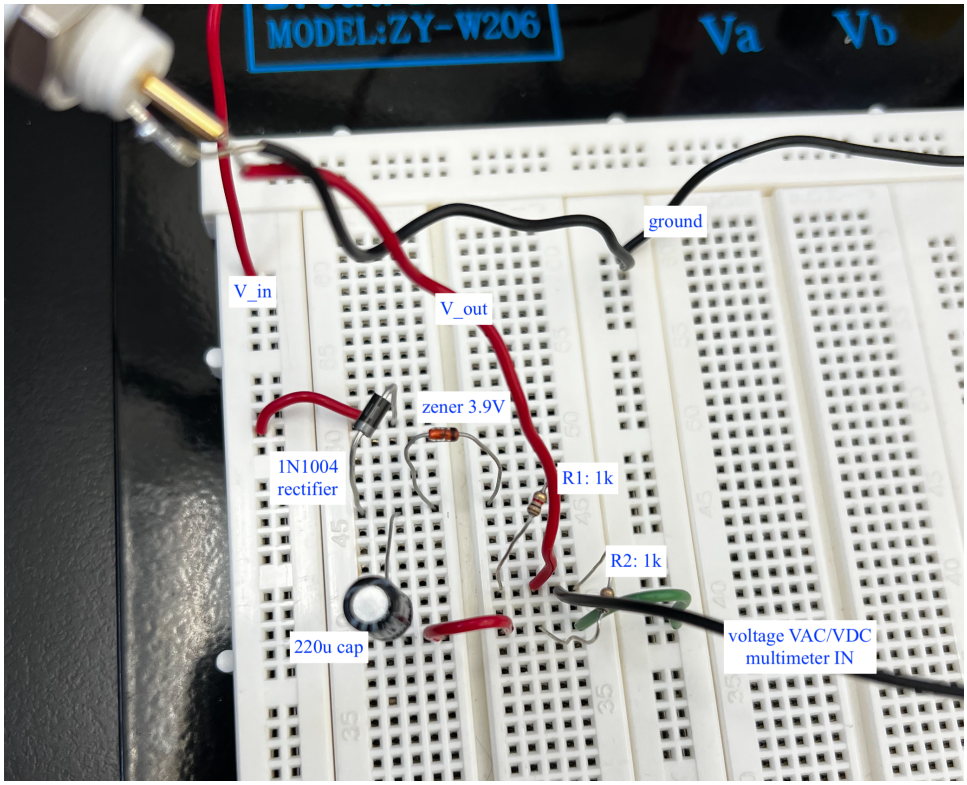

Figure 10: instance of AC to DC converter circuit, as previously modeled in LTSpice.

The DCV was measured to be 4.00 ± 0.05V (it was previously 7.5. The second 1k resistor reduced it to 4), and the ACV was measured to be 23.50 ± 0.05V, which amounts to $> 1\%$ ripple in the output. The V-peak-to-peak measurements on the oscilloscope agreed with that of the multimeter measurements.

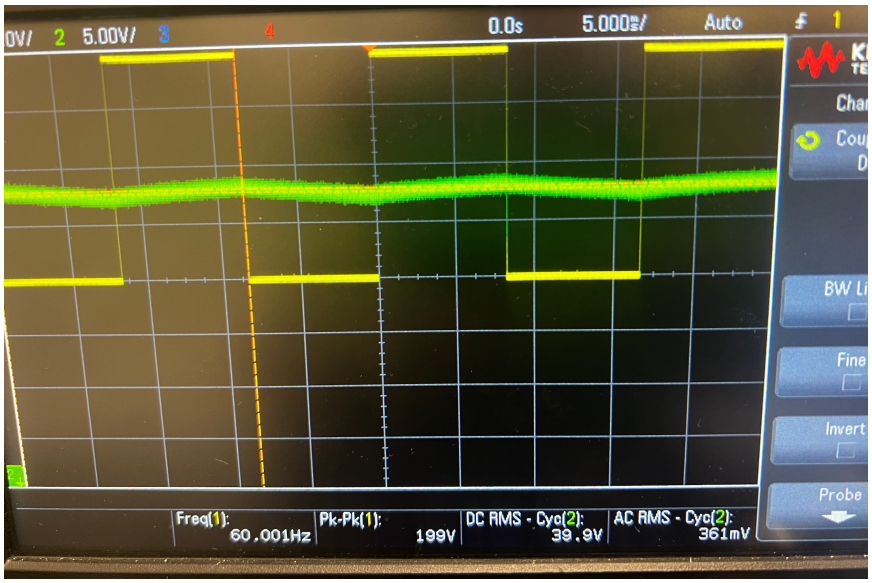

Figure 11: Oscilloscope response of the AC to DC conversion using the circuit designed.

Figure 12: Alternating current voltage measured over the 1k resistor using the multimeter.

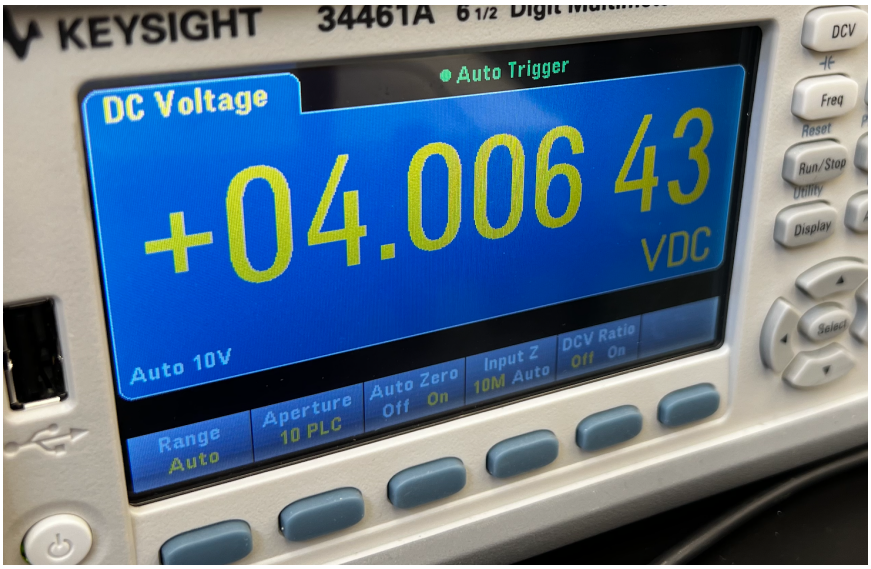

Figure 13: Direct current voltage measured over the 1k resistor using the multimeter.